REMARKS

A. Summary of the Claims

Claims 1-19, 40, and 41 are presently pending. Applicants have (i) amended independent claim 1, (ii) amended dependent claims 3, 5, 7, 9, 11, 13, 15, 17, and 19, and (iii) added new claims 40 and 41. The subject matter of the claim amendments can be found generally throughout the specification, including, but not limited to, paragraphs [0011] and [0036 - 0041] of the published application 2005/0212071. No new matter has been added.

B. Summary of the Non-Final Office Action

In the Non-Final Office Action mailed on July 09, 2008, the Examiner: (i) rejected claims 1, 2, 5, 6, 9, 10, 13, 14, and 17 under 35 U.S.C. § 103(a) as allegedly unpatentable over the combination of U.S. Patent No. 6,429,502 to Librizzi et al. ("Librizzi") and U.S. Patent No. 6,521,947 to ("Ajmera"); (ii) rejected claims 3, 4, 7, 8, 11, 12, 15, and 16 under 35 U.S.C. § 103(a) as allegedly unpatentable over the combination of Librizzi, Ajmera, and U.S. Patent No. 5,264,387 to Beyer et al. ("Beyer"); and (iii) rejected claims 18 and 19 under 35 U.S.C. § 103(a) as allegedly unpatentable over Librizzi, Ajmera, and U.S. Patent No. 5,889,314 to Hirabayashi ("Hirabayashi"). Applicants thank the Examiner for the thorough examination.

C. Response to the Rejections under § 103(a)

Amended claim 1 recites, *inter alia*, "a third guard ring between the first and second guard rings, wherein the third guard ring is in contact with the semiconductor substrate, and wherein the third guard ring is arranged to provide further RF isolation for the first and second semiconductor mesas." Applicants submit that any rejection based on Librizzi and Ajmera necessarily lacks the factual underpinning required to establish *prima facie* obviousness under

MPEP § 2142 for at least the reason that Librizzi and Ajmera, individually or in combination, fail to teach or suggest Applicants' claimed "third guard ring."

First, Librizzi does not teach or suggest Applicants' claimed "third guard ring." Instead, Librizzi shows (i) a first device mesa 28, which is surrounded by isolation trench 26, which is surrounded by guard ring region 36, which is surrounded by isolation trench 24, and (ii) a second device mesa 34, which is surrounded by isolation trench 32, which is surrounded by guard ring region 38, which is surrounded by isolation trench 30. (Librizzi, Fig. 1; col. 4, line 56 - col. 5, line 12.) Indeed, Applicants' review of Librizzi found no teaching or suggestion of "a third guard ring between the first and second guard rings, wherein the third guard ring is in contact with the semiconductor substrate, and wherein the third guard ring is arranged to provide further RF isolation for the first and second semiconductor mesas."

The addition of Ajmera does not overcome the deficiencies of Librizzi because Ajmera, like Librizzi, also fails to teach or suggest Applicants' claimed "third guard ring." Ajmera shows "a contact trench" that "may act as a guard ring." (Ajmera, col. 3, line 67.) Ajmera's "contract trench" does not amount to Applicants' claimed "third guard ring" because Ajmera's "contact trench" is not between any other guard rings, much less a first and second guard ring. Instead of being between two other guard rings, Ajmera's "contact trench" is "patterned…around the [entire] chip in the field area of chip, as illustrated in FIGS. 11 and 12, as represented by 20." (Ajmera, col. 3, lines 29-32.) Indeed, Applicants' review of Ajmera found no teaching or suggestion of "a third guard ring between the first and second guard rings, wherein the third guard ring is in contact with the semiconductor substrate, and wherein the third guard ring is arranged to provide further RF isolation for the first and second semiconductor mesas."

Because Librizzi and Ajmera, whether considered individually or in combination, fail to teach or suggest "a third guard ring between the first and second guard rings, wherein the third guard ring is in contact with the semiconductor substrate, and wherein the third guard ring is arranged to provide further RF isolation for the first and second semiconductor mesas," Applicants submit that any rejection of claim 1 based on Librizzi and Ajmera would necessarily lack the factual underpinnings required to establish *prima facie* obviousness under MPEP § 2142, and that claim 1 is therefore non-obvious and allowable over Librizzi and Ajmera for at least this reason. Applicants further submit that claims 2-19 and 40-41 are likewise allowable over Librizzi and Ajmera for at least the reason that they depend from allowable claim 1.

D. Conclusion

Applicants submit that the present application is in condition for allowance and notice to that effect is respectfully requested. If the Examiner feels that further dialog would advance the application to issuance, the Examiner is invited to telephone the undersigned at 312-913-0001.

Respectfully submitted,

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